Claims

We claim:

1. A system for design and manufacturing verification and enhancement, comprising:

a first enhancement portion for verifying or enhancing a circuit definition to generate a first modified circuit definition with at least one tag, and

a second enhancement portion for verifying and enhancing the second modified circuit definition, wherein:

the first modified circuit definition and the second modified circuit definitions comprise:

one or more geometry representations, and

one or more placement rules;

further comprising an interface between said first enhancement portion and said second enhancement portion, such that said first enhancement portion and said second enhancement portion may be executed independently.

2. The system of claim 1 further comprising:

a storage repository for storing said first enhancement and said second enhancement and storing one or more circuit design rules, one or more circuit design goals and one or more manufacturing specific geometry rules.

3. The system of claim 1 further comprising:

a modification interface for modifying the first enhancement and modifying the second enhancement, and wherein the output of said second modified

circuit definitions at least the structure is modified according to said manufacturing specific geometry rules.

4. The system of claim 1 further comprising:

a data mapper which translates between said circuit definitions and said geometry representations.

5. The system of claim 1 further comprising:

a hierarchical data partitioner for enabling distributed processing by one portion in a processor and a second portion in a second processor.

6. The system of claim 1 further comprising:

said hierarchical data partitioner enables a merging of a plurality of independent layout sub-divisions.

7. The system of claim 1 further comprising:

said manufacturing-specific geometry rules comprise one or more manufacturing process models, or one or more layout enhancement methodologies.

8. The system of claim 1 further comprising:

said one or more circuit design rules and said one or more circuit design goals and said one or more manufacturing-specific geometry rules use a common user interface.

9. The system of claim 8 further comprising:

said circuit design rules, said circuit design goals and said manufacturing-specific geometry rules comprise circuit nets, circuit functions, circuit timing requirements, circuit delay characteristics, the circuit layout and manufacturing-specific process rules.

10. The system of claim 9 further comprising:

said manufacturing-specific process rules use a process rule design chip fabricated by a manufacturer governed by said manufacturing-specific geometry rules.

11. The system of claim 1 further comprising:

said circuit definition comprises a portion of a larger circuit.

12. The method of claim 1 wherein:

said circuit definition comprises one or more circuit and layout files in GDSII, or LEF, or DEF, or Netlist, or MEBES or other proprietary formats.

13. The method of claim 2 wherein:

said storage repository comprises:

a volatile portion and a non-volatile portion.

14. An integrated design verification and manufacturability enhancement tool, comprising:

a physical verification and enhancement platform with an interface to at least one other verification or enhancement engine, and

a common data structure for at least one layout geometry or circuit connectivity engines, and

wherein said platform rule checking for geometric or connectivity operations can be executed sequentially or iteratively.

15. The tool of claim 14 wherein said data structure comprises,

a representation of polygons wherein:

said polygon has a set of vertices and a plurality of pointers associated with other polygons.

16. The tool of claim 15 wherein:

said polygon vertices represent a shape and a location of said polygon.

17. The tool of claim 14 wherein:

said interfaces operate according to a common command script.

18. The tool of claim 14 wherein:

said interfaces comprise a graphical user interface to display data or process flow in a plurality of stages of the physical verification or enhancement process.

19. The tool of claim 14 wherein:

said interfaces comprise a circuit and layout editor which

interactively displays a process flow in one or more stages of the physical verification or enhancement process and enables changing of input data.

20. A method for mask set generation comprising the steps of:

receiving a physical design file comprising the output from an integrated design verification and manufacturability enhancement tool, and

generating a mask set using said physical design file to fabricate an integrated circuit.